REMARKS

This Amendment is responsive to the Final Official Action mailed on August 24, 2004, and is being filed with a Request for Continued Examination. The Office Action again rejected claim 17 under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (U.S. patent number 5,418,752) in view of Kaki et al. (U.S. patent number 5,809,515), with dependent claims 18-22 further rejected in view of Kishi et al. (U.S. patent number 4,841,432) or Noel et al. (U.S. patent publication 2002/00168891). The Office Action also again rejected claims 24-27 under 35 U.S.C. 103(a) as being unpatentable over Fandrich et al. (U.S. patent number 5,509,134) in view of Kishi et al. or Noel et al. For the reasons given below, it is respectfully submitted that various rejections of the pending claims are in error and should be withdrawn. Additionally, as is also discussed below, new claims 28-38 have been added.

Concerning paragraph 2 of the Office Action, this requests that versions 1.0, 1.1, 1.2, and 1.3 of the MultiMediaCard System Specification be supplied. It is unclear why and for what purposes these are being requested. These are not publicly available documents, but rather confidential, internal documents. Additionally, one or more of these requested documents do not even exist. The Office Action provides no motivation for requesting these documents. If the Examiner believes there is some legitimate for requesting these documents, I call to the undersigned is requested to discuss the issue.

Claim 17

The Office Action introduced new grounds for the rejection of claims 17-22, with claim 17 rejected under 35 U.S.C. 103(a) based on Harari in view of Kaki. The final limitation of claim 17 reads:

> wherein *any combination of memory sectors* in a memory group be *simultaneously erased, and any combination of the memory groups* can be *simultaneously erased.*

The emphasis has been added. The Office Action relies upon Kaki to supply these emphasized elements. This is believed to be in error and it is respectfully submitted that the teaching of Kaki are directly contrary to what is found in claim 17.

Rather than teaching that "any combination of memory sectors" and "any combination of the memory groups can be simultaneously erased", the teachings of Kaki are restrictive as to the combinations of erase units that can be set for erasing together. As described at column 7, lines 41-42, "areas to-be-erased are set *so as to be in different memory chips* of the flash

memories 4", where the emphasis has been added. Consequently, Kaki only allows for one unit of erase per chip to set for erase together, whether the appropriate "area to-be-erased" is a sector or a whole chip.

Further, Kaki specifies that the erase of the units of erase are erased *sequentially, not simultaneously*. This is shown in Figure 4 of Kaki and is based on the loop in step 45, as described at column 7, lines 49-50: "Subsequently, the processor 2 determines if the next area to-be-erased exists (step 45)." So that rather than simultaneously erasing all of the units of erase set for erase, Kaki teaches that a sequential process must be used.

In response to this last arguments, the "Response to Amendment" portion of the Office Action states "Kaki discloses simultaneously erasing flash memory sectors (col. 1 line 61 thru col. 2 line 1)." Column 1, line 61, through column 2, line 1, of Kaki reads *in whole* as:

> chip has just begun within the flash memory, and the next data cannot be written until the end of the internal writing operation. Here, a time period of several microsec.~several tens microsec. is expended on the internal writing operation within a flash memory, and it is considerably long compared with the time period, i.e., the actual time used, for writing the command and the data of one word. In this regard, status polling can be utilized as an expedient for

Neither this, nor the adjacent text, present any discussion of erasing, let alone "simultaneously erasing flash memory sectors". It is unclear what the Office Action is referring to and it is again maintained that Kaki specifies that the erase of the units of erase are erased *sequentially, not simultaneously.*

Concerning the use of two levels of tags, the group tags and the sector tags, the cited portion of Kaki states that the erase process described in the preceding discussion is changed according to erase structure used by flash memory; that is, it states that flash memories being used will have a specified unit of erase and that the techniques of the preceding paragraph have to conform with this unit of erase. In the preceding paragraph (beginning at column 7, line 32), this unit of erase is the sector, while in the cited portion (column 7, line 64, through column 8, line 14) the unit of erase is a whole chip. According to Kaki, what the Office Action identifies as "tags" correspond, and can only correspond, to specific unit of erase in the flash architecture. Kaki neither teaches nor suggests the use of two levels of tags for both the basic unit of erase (such as a sector) and the composite, multi-sector unit of the group. Instead, according Kaki, "tags" must correspond to the specific architecture's unit of erase: either sector tags, or rather what the Office Action is identifying as tags, or group tags, but not both.

For any of these reasons, it is believed that a rejection of claim 17 and its dependent claims under 35 U.S.C. 103(a) based on Harari in view of Kaki is not well founded and should be withdrawn. It is respectfully submitted that not only is it is not obvious to combine these two references in the manner recited in the claims, but that the Office Action is improperly combining the two references in a manner gained by hindsight of the present invention and in a manner that is explicitly contrary to the teachings of Kaki.

Claims 18-22 and 24-27

The Office Action rejects claims 18-22 and 24-27 relying upon Kishi et al. or Noel et al. as secondary references. Claims 18-22 have claim 17 as their base claim and are believed allowable for the reasons stated above. It is respectfully submitted that the rejections based upon Kishi or Noel are not well founded and that claims 24-27 are believed allowable and claims 18-22 are believed further allowable for this reason.

More specifically, it is respectfully submitted that neither of these reference are being properly applied by the Office Action. Contrary to what is stated in the Office Action, it appears that neither Kishi nor Noel describes the use of either flash memory in general or memory cells in particular. These references are based on, and all of their teaching are directed to, very different technologies, Kishi is entirely directed at the reconfiguration of *tapes* for controlling machine tools and Noel is directed at multiprocessor computer architectures in which processors and other computer hardware resources are grouped into partitions (specifically, it divides a single physical machine into separate logical partitions to act as independent processors). More specifically, they provide no discussion of "optimizing flash devices" in any form, as stated in the Office Action.

First, considering Kishi, with respect to claims 18, 20, and 24, the Office Action states that "Kishi discloses the number of memory sectors in each memory group is configurable (abstract) for the purpose of optimizing flash devices" and that "Kishi discloses the number of memory cells in each memory sector is configurable (abstract) for the purpose of optimizing flash devices." It is respectfully submitted that both of these statements are incorrect.

The Kishi patent is entirely directed at the reconfiguration of *tapes* for controlling machine tools. It discusses flash devices neither in the abstract nor, as far as can be determined, in the rest of the patent. More specifically, it provides no discussion of "optimizing flash devices" in any form, as stated in the Office Action. Kishi is instead concerned with a very different technology. In particular, there appears to be no disclosure of

a memory system where "the number of memory cells in each memory sector is configurable"---or, for that matter, even the use of memory cells themselves in the technology of Kishi. There also appears to be no disclosure of a memory system where "the number of memory sectors in each memory group is configurable."

Consequently, it is respectfully submitted that a rejection of claim 24 and a further rejection of claims 18 and 20 based on Kishi is not well founded and should be withdrawn. It is believed neither obvious to combine Kishi with the other references nor how to do so; the tape memory of Kishi is a very different technology having a different structure from the sort of memory based on cells and sectors found in the claims.

Claims 19 and 21 respectively depend upon claims 18 and 20 and are believed allowable for the reasons stated above with respect to those claims. Additionally, with respect to claims 19, 21 and 25, the Office Action respectively states "Kishi further discloses the corresponding sectors in each memory group is calculated in real time (col.5 lines 32-42)" and "Kishi further discloses the corresponding cells in each memory sector is calculated in real time (col.5 lines 32-42)." As already noted, Kishi is dealing with a very different technology that would not be obvious to combine with the other reference and which is not based on cells and sectors found in the claims. Consequently, whatever Kishi is up to in the cited location (column 5, lines 32-42), it is neither calculating "number of memory cells in each memory sector" nor "the corresponding sectors in each memory group". Consequently, claim 25 is believed allowable and claims 19 and 21 are further believed allowable for these reasons.

Considering the alternate rejections (or further rejections) based on Noel, with respect to claims 18, 20, and 24, the Office Action states that "Noel discloses the number of memory sectors in each memory group is configurable (block 265) for the purpose of optimizing flash devices" and that "Noel discloses the number of memory cells in each memory sector is configurable (block 265) for the purpose of optimizing flash devices." It is respectfully submitted that both of these statements are incorrect.

The Noel application is directed at multiprocessor computer architectures in which processors and other computer hardware resources are grouped into partitions. Specifically, it divides a single physical machine into separate logical partitions to act as independent processors. The cited location (block 256) is related to a software configuration and mentions memory only to describe the relative privileges that the various logical partitions have to the processors' memory. Noel discusses flash devices neither in this location nor, as far as can be determined, in the rest of the patent. More specifically, it provides no discussion of

"optimizing flash devices" in any form, as stated in the Office Action. Noel is instead concerned with a very different set of problems and technologies. In particular, there appears to be no disclosure of a memory system where "the number of memory cells in each memory sector is configurable"---or, for that matter, even the use of memory cells themselves in the teachings of Noel, as it is concerned with the logical partitions of a machine into independent processors. There also appears to be no disclosure of a memory system where "the number of memory sectors in each memory group is configurable."

Consequently, it is respectfully submitted that the alternate rejection of claim 24 and the further rejection of claims 18 and 20 based on Noel is also not well founded and should be withdrawn. It is believed neither obvious to combine Noel with the other references nor how to do so as the concerns of Noel a very different subject related to multiprocessor computer architectures and having nothing to do with memories based on cells and sectors found in the claims.

Claims 19 and 21 respectively depend upon claims 18 and 20 and are believed allowable for the reasons stated above with respect to those claims. Additionally, with respect to claims 19, 21 and 25, the Office Action respectively states "Noel further discloses the corresponding sectors in each memory group is calculated in real time (block 256)" and "Noel further discloses the corresponding cells in each memory sector is calculated in real time (block 256)." As already noted, Noel is dealing with a very different technology that would not be obvious to combine with the other reference and which is not concerned with cells and sectors as found in the claims. Consequently, whatever Noel is up to in the cited location (block 256), it is neither calculating "number of memory cells in each memory sector" nor "the corresponding sectors in each memory group". Additionally, Noel states that "it is possible to dynamically change partitions", but gives no description of doing this "in real time". Consequently, claim 25 is believed allowable and claims 19 and 21 are further believed allowable for these reasons.

New Claims

New claims 28-38 have been added. As with the currently pending claims, these new claims are all drawn to aspects of the present application described under "IV. ERASE", beginning on line 13 of page 48 and under "V. WRITE PROTECTION", beginning on line 15 on page 52. Many of these claims are based on the aspect of the present inventions that the tags are host settable and, more specifically, that that can both be set and deselected by host

commands. These are further limitations that are not in the prior art and are further reasons these claims are believed allowable.

Conclusion

Therefore, for any of the above reasons it is respectfully submitted that a rejection of claims 17-21 and 23-27 under the stated reasons is not well founded and should be withdrawn. Reconsideration of claims 17-21 and 23-27, along with consideration of new claims 28-38, and an early indication of their allowance are respectfully requested.

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Respectfully submitted,

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